

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Original) A thin film transistor comprising:
2 a buffer layer formed on a substrate;
3 an activation layer formed on said buffer layer; and
4 a gate insulation layer formed on said substrate including said activation layer,
5 with said buffer layer having a step formed between a lower part of said activation layer and
6 a part except said lower part of said activation layer, and said step being a half or less of the
7 thickness sum of said activation layer and gate insulation layer.

1 2. (Original) The thin film transistor according to claim 1, wherein said buffer layer has a
2 step to such a degree that thickness of said gate insulation layer is not changed on said side wall of
3 said buffer layer.

1 3. (Currently Amended) The thin film transistor according to claim 1, wherein a thickness
2 of the gate insulation layer is at least 400 Å when ~~[[the]]~~ a thickness of ~~[[SPC]]~~ solid-phase
3 crystallization polysilicon is 300 Å and step is 350 Å in the activation layer.

1 4. (Currently Amended) The thin film transistor according to claim 1, wherein thickness of
2 the gate insulation layer is at least 1,000 Å when [[the]] a thickness of [[ELA]] excimer laser
3 annealing polysilicon is 500 Å and step is 750 Å in the activation layer.

1 5. (Currently Amended) The thin film transistor according to claim 2, wherein a thickness
2 of the gate insulation layer is 400 Å or more when [[the]] a thickness of [[SPC]] solid-phase
3 crystallization polysilicon is 300 Å and step is 350 Å in the activation layer.

1 6. (Currently Amended) The thin film transistor according to claim 2, wherein thickness of
2 the gate insulation layer is 1,000 Å or more when [[the]] a thickness of [[ELA]] excimer laser
3 annealing polysilicon is 500 Å and step is 750 Å in the activation layer.

1 7. (Withdrawn) A method for fabricating said thin film transistor of claim 1, comprising the
2 steps of:

3 depositing an amorphous silicon layer on a substrate equipped with buffer layer;
4 forming a polycrystalline silicon layer by crystallizing said amorphous silicon layer;
5 forming an activation layer by etching said polycrystalline silicon layer;
6 treating the surface of said activation layer; and
7 depositing a gate insulation layer on said substrate,
8 with etching time being controlled in said activation layer forming process and activation
9 layer surface treatment process so that step between a lower part of gate in the buffer layer and a part

10 except the lower part of said gate has a step value corresponding to a half or less of the thickness sum
11 of said activation layer and gate insulation layer.

1 8. (Withdrawn) The method for fabricating a thin film transistor according to claim 7,
2 wherein the etching time is controlled so that said buffer layer has a step to such a degree that
3 thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

1 9. (Withdrawn) The method for fabricating a thin film transistor according to claim 7,
2 wherein the etching time is controlled to accommodate said buffer layer having a step corresponding
3 to a half or less of the thickness sum of the activation layer and gate insulation layer.

1 10. (Withdrawn) The method for fabricating a thin film transistor according to claim 9,
2 wherein the etching time is controlled so that said buffer layer has a step to such a degree that
3 thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

1 11. (Currently Amended) The method for fabricating a thin film transistor according to claim
2 7, wherein a thickness of said gate insulation layer is 400 Å or more when the thickness of [[SPC]]
3 solid-phase crystallization polysilicon is 300 Å and step is 350 Å in said activation layer.

1 12. (Currently Amended) The method for fabricating a thin film transistor according to claim
2 7, wherein thickness of said gate insulation layer is 1,000 Å or more when the thickness of [[ELA]]

3 excimer laser annealing polysilicon is 500 Å and step is 750 Å in said activation layer.

1 13. (Original) A thin film transistor, comprising:
2 a buffer layer;
3 an activation layer formed on said buffer layer; and
4 a gate insulation layer formed on said buffer layer and said activation layer,
5 with said buffer layer having a step formed between a lower part of said activation layer and
6 a part except said lower part of said activation layer, and said step being up to a half of the thickness
7 sum of said activation layer and gate insulation layer.

1 14. (Original) The thin film transistor according to claim 13, with said step being controlled
2 according to said gate insulation layer being deposited to an even thickness on a side wall of said
3 activation layer.

1 15. (Currently Amended) The thin film transistor according to claim 13, with a thickness of
2 said gate insulation layer being at least 400 Å when ~~[[the]]~~ a thickness of ~~[[SPC]]~~ solid-phase
3 crystallization polysilicon is 300 Å and step is 350 Å in said activation layer.

1 16. (Currently Amended) The thin film transistor according to claim 13, with a thickness of
2 said gate insulation layer being at least 1,000 Å when ~~[[the]]~~ a thickness of ~~[[ELA]]~~ excimer laser
3 annealing polysilicon is 500 Å and step is 750 Å in said activation layer.

1 17. (Withdrawn) A method for fabricating a thin film transistor including a buffer layer, an
2 activation layer formed on said buffer layer, and a gate insulation layer formed on said buffer layer
3 and said activation layer, with said buffer layer having a step formed between a lower part of said
4 activation layer and a part except said lower part of said activation layer, and said step being up to
5 a half of the thickness sum of said activation layer and gate insulation layer, said thin film transistor
6 comprising:

7 forming a polycrystalline silicon layer;

8 forming an activation layer by etching said polycrystalline silicon layer;

9 treating the surface of said activation layer; and

10 depositing a gate insulation layer on said substrate,

11 with etching time being controlled in the activation layer forming process and activation layer
12 surface treatment process to accommodate a step between a lower part of a gate in said buffer layer
13 and a part except the lower part of said gate having a step value corresponding up to a half of the
14 thickness sum of said activation layer and gate insulation layer.

1 18. (Withdrawn) The method for fabricating a thin film transistor according to claim 17,
2 wherein the etching time is controlled to accommodate said buffer layer including the step to such
3 a degree where said gate insulation layer is deposited to an even thickness on a side wall of said
4 activation layer.

1 19. (Withdrawn) The method for fabricating a thin film transistor according to claim 17,
2 wherein the etching time is controlled to accommodate said buffer layer having a step corresponding
3 up to half of the thickness sum of the activation layer and gate insulation layer.

1 20. (Currently Amended) The method for fabricating a thin film transistor according to claim
2 17, wherein a thickness of said gate insulation layer is at least 400 Å when the thickness of [[SPC]]
3 solid-phase crystallization polysilicon is 300 Å and the step is 350 Å in the activation layer or the
4 thickness of said gate insulation layer is at least 1,000 Å when the thickness of [[ELA]] excimer laser
5 annealing polysilicon is 500 Å and the step is 750 Å in said activation layer.